Amendments to the Claims:

1. (original) A delay lock loop circuit for delaying a reference clock to lock a delayed clock, the delay lock loop circuit comprising:

a clock divider for dividing a frequency of the reference clock by N to generate a frequency-divided clock;

a programmable delay circuit electrically coupled to the clock divider, the programmable delay circuit for delaying the frequency-divided clock to generate the delayed clock;

a 180° phase detector electrically coupled to the programmable delay circuit, the 180° phase detector for detecting a phase change of the delayed clock; and

a delay lock loop controller electrically coupled to the programmable delay circuit and the 180° phase detector, the delay lock loop controller for programming the programmable delay circuit to lock the delayed clock according to the phase change.

2. (original) The delay lock loop circuit of claim 1 further comprising a multiplexer electrically coupled to the clock divider and the reference clock, wherein the multiplexer sends either the reference clock or the frequency-divided clock as the driving clock to the 180° phase detector.

3. (original) The delay lock loop circuit of claim 2 wherein if the driving clock is the reference clock, the 180° phase detector is triggered once every N cycles of the reference clock, and if the driving clock is the frequency-divided clock, the 180° phase detector is triggered once each cycle of the frequency-divided clock.

4. (original) The delay lock loop circuit of claim 1 wherein a driving clock of the 180° phase

detector is the frequency-divided clock.

5. (original) The delay lock loop circuit of claim 4 wherein the 180° phase detector is triggered once each cycle of the frequency-divided clock.

6. (original) The delay lock loop circuit of claim 1 wherein a driving clock of the 180° phase detector is the reference clock.

7. (original) The delay lock loop circuit of claim 6 wherein the 180° phase detector is triggered once every N cycles of the reference clock.

8. (withdrawn) A delay lock loop circuit for delaying a reference clock to lock a frequency-divided clock, the delay lock loop circuit comprising:

a programmable delay circuit for delaying the reference clock to generate a delayed clock;

a clock divider electrically coupled to the programmable delay circuit, the clock divider for dividing a frequency of the delayed clock by N to generate a frequency-divided clock;

a 180° phase detector electrically coupled to the clock divider, the 180° phase detector for detecting a phase change of the frequency-divided clock; and

a delay lock loop controller electrically coupled to the programmable delay circuit and the 180° phase detector, the delay lock loop controller for programming the programmable delay circuit to lock the frequency-divided clock according to the phase change.

9. (withdrawn) The delay lock loop circuit of claim 8 wherein a driving clock of the 180° phase detector is the reference clock.

10. (withdrawn) The delay lock loop circuit of claim 9 wherein the 180° phase detector is triggered once every N cycles of the reference clock.

11. (original) A method for delaying a reference clock to lock a delayed clock, the method comprising:

dividing a frequency of a reference clock by N to generate a frequency-divided clock;

delaying the frequency-divided clock by an amount of delay to generate the delayed clock;

providing a 180° phase detector, and utilizing the 180° phase detector for detecting a phase change of the delayed clock; and

programming the amount of delay for locking the delayed clock according to the phase change.

12. (original) The method of claim 11 further comprising selecting the reference clock or the frequency-divided clock to be a driving clock of the 180° phase detector.

13. (original) The method of claim 12 wherein if the driving clock is the reference clock, the 180° phase detector is triggered once every N cycles of the reference clock, and if the driving clock is the frequency-divided clock, the 180° phase detector is triggered once each cycle of the frequency-divided clock.

14. (original) The method of claim 11 wherein a driving clock of the 180° phase detector is the frequency-divided clock.

15. (original) The method of claim 14 wherein the 180° phase detector is triggered once each cycle of the frequency-divided clock.

16. (original) The method of claim 11 wherein a driving clock of the 180° phase detector is the reference clock.

17. (original) The method of claim 16 wherein the 180° phase detector is triggered once every N cycles of the reference clock.

18. (withdrawn) A method for delaying a reference clock to lock a frequency-divided clock, the method comprising:

delaying a reference clock by an amount of delay to generate a delayed clock;

dividing a frequency of the delayed clock by N to generate the frequency-divided clock;

providing a 180° phase detector, and utilizing the 180° phase detector for detecting a phase change of the frequency-divided clock; and

programming the amount of delay for locking the frequency-divided clock according to the phase change.

19. (withdrawn) The method of claim 18 wherein a driving clock of the 180° phase detector is the reference clock.

20. (withdrawn) The method claim 19 wherein the 180° phase detector is triggered once every N cycles of the reference clock.

21. (new) A delay lock loop circuit comprising:

a clock divider and programmable delay circuit for dividing a frequency of a reference clock by N and delaying the frequency to thereby generate a delayed and frequency-divided

clock;

a 180° phase detector electrically coupled to the clock divider and programmable delay circuit, the 180° phase detector for detecting a phase change of the delayed and frequency-divided clock; and

a delay lock loop controller electrically coupled to the clock divider and programmable delay circuit, and the 180° phase detector; the delay lock loop controller for programming the clock divider and programmable delay circuit to lock the delayed and frequency-divided clock according to the phase change.

22. (new) A method for delaying a reference clock, the method comprising:

dividing a frequency of a reference clock by N and delaying the reference clock by an amount of delay to thereby generate a delayed and frequency-divided clock;

providing a 180° phase detector, and utilizing the 180° phase detector for detecting a phase change of the delayed and frequency-divided clock; and

programming the amount of delay for locking the delayed and frequency-divided clock according to the phase change.